METHOD AND APPARATUS FOR PROVIDING A GIGABIT ETHERNET CIRCUIT PACK

Inventors: Anthony William Jorgenson
39533 Platero Pl.
Fremont, CA 94539
U. S. Citizen

Nicholas Joseph Possley
6351 Snowberry Ct.
Gilroy, CA 95020
U.S. Citizen

RELATED APPLICATION

This application claims priority under 35 USC §119 to provisional application no. 60/269,225 entitled "Method and Apparatus for Providing a Gigabit Ethernet Circuit Pack" filed on February 14, 2001, and to provisional patent application entitled "System and Method for Recovering RZ Formatted Data Using NRZ Clock and Data Recovery," having inventors Nicholas J. Possley and David B. Upham, filed May 9, 2001, the disclosures of each of is incorporated herein by reference for all purposes.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to data network systems. In particular, the present invention relates to method and apparatus for providing transparently transporting 155 Mb/s signals through a high speed data network.

2. Description of the Related Art

Optical fiber is a transmission medium that is well suited to meet the increasing demand in data transmission in communication networks. Generally, optical fiber has a much greater bandwidth than metal-based transmission medium such as twisted copper pair or coaxial cable, and protocols such as the OC protocol have been developed for the transmission of data over optical

fibers. Typical communications system based on optical fibers include a transmitter, an optical fiber, and a receiver. The transmitter converts the data to be transported into an optical form using the proper protocol and then transmits the resulting optical signal over the optical fiber to the receiver, where the original data is recovered from the optical signal.

While adding more optical fiber to the existing communications network infrastructure is a costly option to meet the increasing demand for communication bandwidth, in some locations, expanding the existing network may not be a viable alternative. Additionally, given the high cost of installation and the extensive amount of time required, adding more optical fiber is not always an attractive option to increase communications bandwidth.

Due to the large bandwidth capability of optical fibers, this type of transmission medium is most efficiently utilized when multiple users share the medium. In general, a number of low-speed data streams ("low speed channels") transmitted by different users may be combined into a single high-speed channel for transporting across the optical fiber medium. At the opposite end of the communications network, when the high-speed channel reaches the destination for one of the low-speed channels that it is transporting, the low-speed channel must be extracted from the high-speed channel.

A typical optical communications network includes nodes (for example, central offices) which transmit high-speed channels to each other over optical fibers. In addition to transporting low-speed channels through the nodes (commonly referred to as the "pass-through" function) as part of high-speed channels passing through the nodes, nodes may also combine incoming low-speed channels to the high-speed channel (i.e., the "add" function) and/or extract outgoing low-speed channels from the high-speed channels (the "drop" function). These functions are commonly referred to as add-drop multiplexing (ADM).

For example, wavelength division multiplexing (WDM) and time division multiplexing (TDM) are two known approaches to combining low-speed channels into a high-speed channel. In WDM and its counterpart dense

wavelength division multiplexing (DWDM), each low-speed channel is placed on an optical carrier of a different wavelength and the different wavelength carriers are combined to form the high-speed channel. Crosstalk between the low-speed channels is a significant concern in WDM, and thus the wavelengths for the optical carriers must be spaced sufficiently far apart (typically 50 GHz or more) so that the different low-speed channels are resolvable.

In TDM, each low-speed channel is compressed into a certain time slot and the time slots are then combined on a time basis to form the high-speed channel. For example, given a certain period of time, the high-speed channel may be capable of transporting 10 bits while each low-speed channel may only be capable of transmitting 1 bit. In this case, the first bit of the high-speed channel may be allocated to low-speed channel 1, the second bit to low-speed channel 2, and so on, thus forming a high-speed channel containing 10 low-speed channels. Generally, TDM requires precise synchronization of the different channels on a bit-by-bit basis (or byte-by-byte basis, in the case of SONET), and a memory buffer is typically also required to temporarily store data from the low-speed channels.

SUMMARY OF THE INVENTION

In view of the foregoing, a method of transporting data through a data network, in accordance with one embodiment of the present invention includes the steps of receiving an encoded data, mapping the received data to a predetermined data; and multiplexing the mapped predetermined data.

In particular, the encoded data may be an 8B/10B encoded data which includes either a Gigabit Ethernet data and a Fiber Channel data.

The receiving step may further include the step of determining a data rate of the received encoded data, and the step of recovering a clock signal from the received encoded data.

The clock signal may have a rate one tenth of said data rate, where the predetermined data may include a 9-bit data. In turn, the 9-bit data may include one of an arbitrary set of 9-bit data.

The multiplexing step may include the step of synchronizing the multiplexed predetermined data, where the multiplexed predetermined data may be synchronized to a predetermined clock signal, and further, where the predetermined clock signal may include a phase locked loop clock signal.

An apparatus for providing data transport through a data network in accordance with another embodiment of the present invention includes a clock recovery unit configured to receive an encoded data, a data translation unit coupled to the clock recovery unit, configured to translate the received data to a predetermined data, and an inverse multiplexer coupled to the data translation unit, configured to inverse multiplex the translated predetermined data.

The encoded data may include 8B/10B encoded data, and in particular, one of a Gigabit Ethernet data and a Fiber Channel data.

The clock recovery unit may additionally detect a data rate of the received encoded data, and further, the clock recovery unit may be further configured to recover a clock signal from the received encoded data.

The clock signal may have a rate one tenth of said data rate.

Additionally, the predetermined data may include a 9-bit data, where the 9-bit data may include one of an arbitrary set of 9-bit data.

The inverse multiplexer may be further configured to synchronize the multiplexed predetermined data to a predetermined clock signal, where the predetermined clock signal may include a phase locked loop clock signal.

Additionally, a modem may be coupled to the inverse multiplexer to receive the inverse multiplexed translated predetermined data for transmission.

The inverse multiplexed translated predetermined data may include a plurality of STS-3 signals, where the plurality of STS-3 signals may include eight STS-3 signals for transmission.

An apparatus for providing data transport in a network in accordance with yet another embodiment of the present invention includes a demultiplexer configured to demultiplex received data, a data translation unit coupled to the multiplexer configured to translate the demultiplexed data to a predetermined data, and a serializer coupled to the data translation unit configured to receive

the translated predetermined data and accordingly to generate a corresponding encoded data.

The received data may include a plurality of STS-3 signals, where the plurality of STS-3 signals may include eight STS-3 signals.

Additionally, a plurality of FIFOs may be provided, each configured to frame align the STS-3 signals, the frame aligned STS-3 signals corresponding to the received signal.

The demultiplexed data may include a 9-bit data, where the 9-bit data may have a data rate of 1,125 Mbits/second.

The demultiplexer may be further configured to perform parity checks on the received data.

The predetermined data may include a 10-bit data.

The serializer may be configured to synchronize the translated predetermined data, where the translated predetermined data may include a 10-bit data, and further, where the10-bit data may have a data rate of 1,250 Mbits/second.

The encoded data may include an 8B/10B encoded data.

A method for providing data transport in a network in accordance with still another embodiment of the present invention includes the steps of demultiplexing a received data, translating the demultiplexed data to a predetermined data, generating a corresponding encoded data based on the translated predetermined data.

The received data may include a plurality of STS-3 signals, where the plurality of STS-3 signals may include eight STS-3 signals.

The method may further include the step of frame aligning each of the STS-3 signals, the frame aligned STS-3 signals corresponding to the received data for demultiplexing.

The demultiplexed data may include a 9-bit data, where the 9-bit data may have a data rate of 1,125 Mbits/second.

Additionally, the method above may further include the step of performing parity checks on the received data, as well as the step of

synchronizing the translated predetermined data.

The translated predetermined data may include a 10-bit data, where the 10-bit data may have a data rate of 1,250 Mbits/second.

Finally, the encoded data may include an 8B/10B encoded data.

In the manner described, the present invention discloses method and system for providing data transmission with transparency over the Gigabit Ethernet as well as other data stream which includes receiving the 10 bit code with a data rate of 1,250 Mbits/second from the encoded 8B/10B data and arbitrarily selecting 9 bit codes using a look-up translation table which can fully represent the 10 bit codes received. The translated 9 bit codes with a data rate of 1,125 Mbits/second is then provided to eight STS-3 inverse multiplexer which inverse multiplexes the received codes into eight STS-3 data streams each with a data ate of 155.52 Mbits/second which are then provided to the modulator at the near end and demodulator at the far end.

These and other features and advantages of the present invention will be understood upon consideration of the following detailed description of the invention and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates an overall system in the add direction in accordance with one embodiment of the present invention.

Figure 2 illustrates the overall system shown in Figure 1 in the drop direction in accordance with one embodiment of the present invention.

Figure 3 illustrates an overall system configured for transporting OC-48 optical signals in the add direction in accordance with one embodiment of the present invention.

Figure 4 illustrates the overall system shown in Figure 3 in the drop direction in accordance with one embodiment of the present invention.

Figure 5 is a tabular illustration of a pseudo STS-3 frame for use in multiplexing Gigabit ethernet data in the overall system shown in Figures 1-4.

Figure 6 is a tabular illustration of a pseudo STS-3 frame for use in

multiplexing Fiber channel data.

Figure 7 is a tabular illustration of a pseudo STS-3 frame for use in multiplexing RZ data.

Figure 8 illustrates frame byte definitions for pseudo STS-3 frames shown in Figures 5-7.

Figure 9 illustrates a pseudo STS-3 configurable frame that can multiplex data at any rate in accordance with another embodiment of the present invention.

Figure 10 illustrates a table showing the configuration parameters for each data rate for the configurable frame of Figure 9.

Figure 11 illustrates frame byte definitions for the configurable frame of Figure 9.

Figure 12 illustrates a flowchart for providing data translation in the add direction in accordance with one embodiment of the present invention.

Figure 13 illustrates a flowchart for providing data translation in the drop direction in accordance with one embodiment of the present invention.

DETAILED ESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 1 illustrates an overall system in the add direction in accordance with one embodiment of the present invention. Referring to Figure 1, in the overall system 100, there is provided a clock recovery unit 110, a data translation unit 120, an STS-3 inverse multiplexer 130, and a phase-lock loop (PLL) unit 150. Furthermore, the data translation unit 120 includes a 10 bit-to-9 bit translation table 121. In one aspect of the present invention, 8B/10B encoded data is provided to the clock recovery unit 110. For example, both Gigabit Ethernet and Fiber Channel signals are encoded using the 8B/10B encoding scheme. In particular, under this coding scheme, 8 data bits are translated into 10 bits for the purpose of transition density of data for the clock recoveries and parity information for additional error detection.

Referring back to Figure 1, in one embodiment, the clock recovery unit 110 is configured to recover clock signals from the received encoded data and

to provide the recovered clock signal to the data translation unit 120 and the PLL unit 150. Moreover, the clock recovery unit 110 is also configured to provide the 10-bit data with a data rate of 1,250 Mbits/second to the data translation unit 120. As shown, the clock signal from the clock recovery unit 110 in one embodiment may be at a tenth of the data rate of the encoded data received. Moreover, in one aspect of the present invention, the clock recovery unit 110 may be configured to receive the 8B/10B encoded data without a clock signal, and to derive a clock signal using a phase lock loop (PLL) within the clock recovery unit 110. The derived clock signal may then be used in the digital components of the overall system 100 to sample and process the data. Indeed, in one aspect, the PLL unit 150 may be configured to frequency translate the incoming clock frequency to a predetermined frequency to derive a synchronous 155.52 MHz OC-3 clock that may be used to interface with the system 100.

As further shown, the data translation unit 120 is configured to translate the received 10-bit data to a corresponding 9-bit data. In particular, the system 100 queries the translation table 121 to determine the 9-bit data corresponding to the received 10-bit data. In one aspect of the present invention, the 10-bit to 9-bit translation table 121 of the data translation unit 120 may include 464 unique 9-bit codes, each corresponding to a separate one of the received 10-bit data. Moreover, the 9-bit codes may be arbitrarily chosen. Additionally, as shown in the Figure, 10 bit data received from clock recovery unit 110 which do not require translation is passed through the data translation unit 120 which uses the translation table 121 to determine whether the received data bit code is valid, and outputs the valid confirmed 10 bit data to the 8xSTS-3 inverse multiplexer 130.

Furthermore, as will be discussed below, any 10-bit data received which does not map to one of the 464 9-bit codes in the translation table 121 may result in a /V/ code translation indicating an error. It should be noted that /V/ codes are 10-bit codes defined by IEEE to be used for error propagation. In particular, /V/ codes are inserted as data in the STS-3 frame when a LOSYN

defect or LOS defect exists on the add direction input. In particular, in the case of Gigabit Ethernet or Fiber Channel data streams, for a LOSYN defect, as soon as a comma is detected, the /V/ code insertion ceases.

The translated 9-bit data with a data rate of 1,125 Mbits/second is provided to the inverse multiplexer 130 which, along with the phase lock looped clock signal from the PLL unit 150, inverse multiplexes the received 9-bit data into corresponding STS-3 signals. In one aspect, the phase lock looped clock signal from the PLL unit 150 is at 155.52 MHz with an offset Δ, where the offset Δ is a 20 ppm (parts per million) or less offset. Indeed, with the incoming bit data determined, the PLL unit 150 locks onto the incoming data rate. An ADD PLL alarm may be configured to indicate the status of the PLL unit 150 - whether the PLL unit 150 is in locked or unlocked state. This permits the overall system to maintain the timing on the clock instead of the data. Furthermore, in another embodiment, variable bit stuffing may be implemented as will be discussed in further detail below. With both cases, since the add direction clock signal is locked onto the incoming data, the data will fit exactly into the data frames shown in Figures 5-7 discussed in further detail below.

Moreover, in addition to inverse multiplexing the 9-bit data into eight STS-3 signals, the inverse multiplexer 130 is further configured to provide variable byte stuffing. Then, the eight STS-3 signals, each at a data rate of 155.52 Mbits/second + offset Δ with all eight STS-3 signals synchronized and frame aligned, are provided to a modem 140 for transmission via the optical transmission line to the drop side. In particular, the modem 140 includes eight modulators one for each STS-3 signal output from the STS-3 inverse multiplexer 130. More specifically, each of the eight modulators together comprising the modem 140 is similar to modulator as described in pending U.S. Patent Application No. 09/571,349, filed May 16, 2000 by inventors David A. Pechner and Laurence J. Newell entitled "Through-Timing of Data Transmitted Across an Optical Communications System Utilizing Frequency Division Multiplexing" assigned to the assignor of the present application, and the disclosure of which is incorporated herein by reference for all purposes.

As discussed above, in accordance with one embodiment of the present invention, 8B/10B encoded data which includes, for example, Gigabit Ethernet and Fiber Channel signals, may be fully represented by 9 bits and may be transported transparently to ensure that parity and special code functions are passed on to the customers. Furthermore, in one aspect of the present invention, the PLL unit 150 and the clock recovery unit 110 may be configured to permit the overall system 100 to "tune" to each of the signal rates, such as, for example, in the case of Gigabit Ethernet data whose rate is approximately 1,250 Mb/s encoded and approximately 1,000 Mb/s decoded.

Figure 2 illustrates the overall system shown in Figure 1 in the drop direction in accordance with one embodiment of the present invention. Referring to Figure 2, there is provided STS-3 multiplexer/9-bit demultiplexer 220 which is configured to receive eight STS-3 signals from modem 210. The modem 210 is similar to the modem 140 described above in Figure 1 in the add direction of the communication path. Further shown in Figure 2 is a data translation unit 230 coupled to the STS-3 multiplexer/9-bit demultiplexer 220, as well as a phase lock loop (PLL) unit 250 and a serializer 240. The serializer 240 may be provided with translated 10 bit data from the data translation unit 230 along with phase lock looped clock signal from the PLL unit 250 to regenerate the 8B/10B encoded data. Coupled between the modem 210 and the STS-3 multiplexer/9-bit demultiplexer 220 is a FIFO 260 which is configured to receive the eight STS-3s for frame aligning. In particular, under the control of a frame aligning state machine, FIFO 260 which in one embodiment includes eight separate FIFOs for each of the received STS-3s, is configured to frame align each received STS-3s to line up the STS-3s which are received from the modem 210 with slight delay.

In particular, in accordance with one aspect of the present invention, the STS-3 multiplxer/9-bit demultiplexer 220 may be configured to perform parity checks and to demultiplex the 9 bits from the received eight STS-3 signals. The recovered 9-bit data with a data rate of 1,125 Mbits/second is then provided to the data translation unit 230 which includes a 9-bit-to-10-bit translation table

231. In one embodiment, the system 200 may be configured to retrieve a corresponding 10-bit data for the recovered, received 9-bit data from the STS-3 multiplexer/9-bit demultiplexer. As will be discussed in further detail below, in one embodiment, the 9-bit to 10-bit translation table 231 of the data translation unit 230 may be a look-up table stored in the data translation unit 230 under the control of a controller (not shown) of the data translation unit 230. In particular, the translation table 231 may be, in one embodiment, stored in a storage unit within the data translation unit 230, where the storage unit may include a memory such as a random access memory.

Referring back to Figure 2, the PLL unit 250 is configured to receive a 19.44 MHz clock signal from the STS-3 signal transmission from the modem 210, and is configured to recover a clock signal at a tenth of the data rate to provide the clock signal to the serializer 240, as well as to the data translation unit 230 and the STS-3 Multiplxer/9-bit demultiplexer 220. As discussed above, the serializer 240 is configured to synchronize the translated 10-bit data with a data rate of 1,250 Mbits/second received from the data translation unit 230 with the clock signal received from the PLL unit 250 and to regenerate the 8B/10B encoded data. In this manner, in accordance with one embodiment of the present invention, in the drop direction, the 8B/10B encoded data may be recovered from the received eight STS-3 signals.

Figure 3 illustrates an overall system configured for transporting OC-48 optical signals in the add direction in accordance with one embodiment of the present invention. Referring to Figure 3, there is provided a pair of Clock and Data Recovery (CDRs) 310 each configured to receive Gigabit ethernet data. Also shown in Figure 3 are Deserializer (DES) 320 configured to receive the data and the clock signal from the corresponding CDR 310 and output a 10-bit data each. The clock signal from the CDR 310 is also provided to the divider 330 which is configured to divide the clock signal from the CDR 310 by a factor of 10. The 10-bit data from the DES 320 is provided to the 10-bit to 9-bit translation unit 340 which is configured to translate the 10-bit data received from the DES 320 into a respective corresponding 9-bit data. The 9-bit data

from each 10-bit to 9-bit translation unit 340 is then provided to the elastic store unit 350. The elastic store 350 in one embodiment is configured to perform buffering of the data during the time the multiplexer is transmitting frame overhead or bit stuffing.

As further shown in Figure 3, the clock signal divided by the divider 330 is provided to the 10-bit to 9-bit translation unit 340 as well as to the elastic store unit 350. The 9-bit data from the elastic store unit 350 is provided to STS-48c Mapper/Scrambler 360 which is also configured to receive a clock signal from the multiplexer clock 370. As further shown, the multiplexer clock is also provided to each elastic store units 350. Additionally, the STS-48c Mapper/Scrambler 360 is also configured to receive overhead data from the STS-48c overhead generator 380 as well as a 155.52 MHz clock signal. The 16-bit STS-48c data output from the STS-48c Mapper/Scrambler 360 is then provided to serializer/optical transceiver 390 which is then configured to transmit OC-48c data to the remote side.

Figure 4 illustrates the overall system shown in Figure 3 in the drop direction in accordance with one embodiment of the present invention. Referring to Figure 4, OC-48c signal is received by CDR/Optical transceiver 410 which is configured to output 16-bit STS-48c data to the STS-48c LTE/PM Demultiplexer/descrambler 420. The CDR/optical transceiver 410 is also configured to transmit a 155.52 MHz clock signal to the STS-48c LTE/PM Demultiplexer/descrambler 420.The 9-bit data output from the STS-48c LTE/PM Demultiplexer/descrambler 420 is provided to respective FIFO leak buffer 430. The FIFO leak buffer 430 are also configured to receive the 155.52 MHz clock signal from the CDR/optical transceiver 410.

The frame aligned 9-bit data from the respective FIFO leak buffer 430 is the provided to the respective elastic store units 440. More particularly, the FIFO leak buffer 430 is configured to send the 155.52 clock signal in addition to the 9-bit data. The elastic store unit 440 is also configured to receive the 9-bit data from the FIFO leak buffer 430. The 155.52 MHz clock signal from the FIFO leak buffer 430 is also provided to the respective elastic store units 440 as

well as to a logical OR 490.

Referring back to Figure 4, as can be seen, the output of the O R 490 which is a gapped clock signal, is provided to the dynamic phase locked loop (DPLL) 450 whose output is provided to the elastic store unit 440, the 9-bit to 10-bit translation unit 460 and to the PLL multiplier 470. The multiplication factor for the PLL multiplier 470 may in one embodiment include ten. As can be further seen from Figure 4, the 9-bit data provided from the elastic store unit 440 to the 9-bit to 10-bit translation unit 460 is translated and output as a corresponding 10-bit data. The 10-bit data from the 9-bit to 10-bit translation unit 460 as well as the output from the PLL multiplier 470 is provided to the SER 480 which is configured to output gigabit ethernet data from the received information. In this manner, in accordance with one embodiment of the present invention, in the drop direction of a data transmission scheme, the data may be transported transparently in the data network.

Figure 5 is a tabular illustration of a pseudo STS-3 frame for use in multiplexing Gigabit ethernet data in the overall system shown in Figures 1-4. Referring to Figure 5, as can be seen, the Gigabit ethernet data pseudo STS-3 frame table 500 substantially corresponds to the STS-3 inverse multiplexer 130 of the overall system 100 shown in Figure 1. Indeed, as shown, each of the eight sets of 9-bit codes is multiplexed into a pseudo STS-3 frame as shown in the Gigabit ethernet data pseudo STS-3 frame table 500. As can be seen from Figure 5, the number of bits in each row of the Gigabit ethernet data pseudo STS-3 frame table 500 is equivalent to the number of bits in a row of an STS-3 signal since it has to run at the same data rate. The byte definition for each entry in the Gigabit ethernet data pseudo STS-3 frame table 500 can be seen in Figure 8 which will be discussed in further detail below.

Figure 6 is a tabular illustration of a pseudo STS-3 frame for use in multiplexing fiber channel data. Referring to Figure 6, as can be seen, the fiber channel data pseudo STS-3 frame table 600 substantially corresponds to the STS-3 inverse multiplexer 130 of the overall system 100 shown in Figure 1. In particular, the fiber channel data pseudo STS-3 frame table 600 of Figure 6

illustrates the pseudo STS-3 frame in the case of Fiber Channel signals. In particular, if the data is Fiber Channel data, the 10-bit codes are passed through with no translation since the data rate is much less as compared with the case where the data is Gigabit Ethernet. Indeed, the 10-bit codes are inverse multiplexed into eight sets of 10-bit codes and multiplexed in to the pseudo STS-3 frame of Figure 6. Again, the byte definition for each entry in the translation table 600 of Figure 6 can be seen in Figure 8.

Figure 7 is a tabular illustration of a pseudo STS-3 frame for use in multiplexing VRH-RZ (Variable Rate High Speed-RZ) data. Referring to Figure 7, for the 1,129.984 Mb/s RZ signal, the data is multiplexed into the pseudo STS-3 frame for VRH-RZ data table 700 shown in Figure 7 in blocks of 10-bits at 112.9984 MHz. For the 564.992 Mb/s signal, the data is multiplexed into the pseudo STS-3 frame for VRH-RZ data table 700 shown in Figure 7 in blocks of 5-bits at 112.9984 MHz. This allows the same clock and logic structure to be reused. Again, the byte definition of each of the entries in the pseudo STS-3 frame for VRH-RZ data table 700 of Figure 7 can be found in Figure 8. A skilled artisan would have available a variety of methods to interface to RZ signals, several approaches of which are disclosed in pending application entitled, "System and Method for Recovering RZ Formatted Data Using NRZ Clock and Data Recovery," having inventors Nicholas J. Possley and David B. Upham, filed on May 9, 2001.

Figure 8 illustrates frame byte definitions for the pseudo STS-3 frames shown in Figures 5-7. Referring to Figure 8, the byte definition table 800 includes a corresponding definition of each byte entry of the pseudo STS-3 frame tables 500, 600, and 700 shown in Figures 5-7, respectively for Gigabit ethernet data, fiber channel data and VRH-RZ data, as well as their corresponding value. For example, bytes A1 and A2 corresponds to the framing byte with values of 0xF6 and 0x28, respectively. Moreover, bytes R, R1, and R2 correspond to the 8 bit fixed stuff, 9 bit fixed stuff and 10 bit fixed stuff, respectively, having values of 0xFF, 0x1FF and 0x3FF, respectively.

Referring back to Figures 5-7, as can be seen, the STS-3 frames are

scrambled using the standard SONET scrambler and sent to the modem 140 (Figure 1). Further, the frame contains fixed stuff bytes and variable stuff bytes which are included due to data rate mismatch. Additionally, the STS-3 frames shown in Figures 5-7 contain parity BIP-8 bytes used for performance monitoring and establishing Signal Degrade conditions over the data link. In particular, the parity is determined over each pseudo STS-1 within each of the pseudo STS-3s. Moreover, as can be seen, the frame also contains ID bytes which are used to authenticate the source of the data and order. In particular, if the order or authentication does not match, then a cross-connect fault may be declared on the drop side. Additionally, the frame further contains an Alarm Notification Signal (ANS) byte which is used to indicate to the far end drop-side that there is a near end add-side defect. Furthermore, for fault isolation, LOS defect may be accumulated to provide a LOS fault, while LOL may be accumulated to provide a LOL fault.

Figure 9 illustrates a configurable STS-3 frame for a VRVH (Variable Rate Very High) circuit pack in accordance with another embodiment of the present invention, while Figure 10 illustrates a table showing the configuration parameters for each data rate for the configurable STS-3 frame of Figure 9.

In one embodiment, the VRVH circuit pack is configured to support non-standard signals in the range from 565 Mb/s to 1,184.265 Mb/s. In particular, the STS-3 frame shown in Figure 9 has the same number of bits per frame as an STS-3 data which is 2,160 bits per row. Furthermore, the VRVH circuit pack may be configured to provide the functionality of transparently transporting the non-standard signals through the data network system. The data network system may be through-timed from the input signals, with the data being multiplexed into the STS-3 frame shown in Figure 9. Furthermore, as shown, Figure 10 illustrates the frame parameters for the various signal types as applied to the STS-3 frame shown in Figure 9.

Figure 11 illustrates frame byte definitions for the frame for the STS-3 and the corresponding data rate for the various signal types as shown in Figure 9-10, respectively. Referring to the figure, it can be seen that, for example,

bytes A1 and A2 correspond to framing bytes with values of 0xF6 and 0x28, respectively. Moreover, bytes R(0), R(1), and R(2) correspond to 8, 9 and 10 bit fixed stuff having values of 0xFF, 0x1FF, and 0x3FF, respectively. Furthermore, referring back to Figure 10, the NEC1.12 parameters were selected based upon an 8KHz frame rate, and due to the PLL divider limitations, the frame rate may be slightly different.

Figure 12 illustrates a flowchart for providing data translation in the add direction in accordance with one embodiment of the present invention. Referring to Figure 12, in the add direction, at step 1210, the 8B/10B encoded data is received. Thereafter at step 1220, the clock signal from the received data is recovered and the data rate is detected. At step 1230, the 10-bit data is mapped to corresponding 9-bit code using a look-up table as shown in Figure 1, and at step 1240, the 9-bit code is inverse multiplexed to corresponding pseudo STS-3 signals which are synchronized to the clock signal of the encoded data received at step 1210.

Figure 13 illustrates a flowchart for providing data translation in the drop direction in accordance with one embodiment of the present invention. Referring to Figure 13, at step 1310, a plurality of STS-3 signals are received and at step 1320, the received STS-3 signals are multiplexed into 9-bit data. Thereafter at step 1330, the multiplexed 9-bit data is mapped to corresponding 10-bit data. Finally, at step 1340, the 8B/10B encoded data corresponding to the 10-bit data is regenerated after being synchronized with the received STS-3 signals.

As discussed above, in accordance with one embodiment of the present invention, in the add direction, the Gigabit Ethernet, RZ signals, or Fiber Channel data is inverse multiplexed into eight pseudo STS-3 data streams. The data network system 100 then modulates and sums the data stream with all other data streams for transport over an optical fiber connection. At the far end, the data network system 100 receives the eight pseudo STS-3 signals from the modem 140 and multiplexes the data back into the original high speed data stream. Pending U.S. Patent Application entitled "Variable Rate High-Speed

Input and Output in Optical Communication Network," having inventors Tian Shen, Robert B. Clarke, Jr., Thomas J. Roman, David B. Upham, David A. Pechner, and Laurence J. Newell, filed on May 8, 2001, and assigned to the assignee of the present application, Kestrel Solutions, Inc., provides additional examples of variable rate high speed input and output in an optical network using optical frequency division multiplexing, the disclosure of which is incorporated in its entirety by reference for all purposes.

In the drop direction, the data network system 100 may be configured to receive both sets of eight data streams from each of the drop cross- connects. Accordingly, SONET framers may be used to frame-up each of the pseudo STS-3s, with the delay compensated for between each of the pseudo STS-3's in each set of eight data streams. It should be noted that the delay is compensated for between the pseudo STS-3's in a set. In one aspect, the maximum delay between any pseudo STS-3 is approximately 26.3 μs. Since this delay value is much less than the frame period of approximately 125 μs, the alignment of the pseudo STS-3's may occur where the framing pulses are nearest to each other. Moreover, it should be noted that in both the add and drop directions, the system 100 may be configured to perform a predetermined level of performance monitoring and fault detection on the data stream.

In one aspect of the present invention, a Gigabit Ethernet Circuit Pack proposed by the assignee of the present invention, Kestrel Solutions, is configured to provide an additional interface added to the low speed shelf, the added interfaces including 1250 Mbps Gigabit Ethernet, 1062.5 Mbps Fiber Channel, 1129.984 Mb/s Return-to-Zero (RZ) data and 564.992 Mbps RZ data. The circuit pack is thus configured to provide the functionality of transparently transporting these signal formats through the backend of a data network which is through-timed from the input signals.

In particular, as discussed above, since both the Gigabit Ethernet and the Fiber Channel signals are encoded using the 8B/10B encoding scheme, the 8 bits are transmitted into 10 bits for the purpose of transition density of data for the clock recoveries and parity information for additional error detection.

Indeed, since the 8 bits are mapped into two sets of 10-bit codes, the two sets providing the parity information, it can be seen that only a maximum of 512 different codes need be used. Furthermore, by examining the code table in IEEE 802.3 publication, it can be seen that 72 of the 512 codes are duplicates, which leaves 440 codes for the data. Additionally, apart from the data, IEEE 802.3 publication defines 12 special codes used for various functions such as start-of-packet, error propagation, end-of-pocket, idle, and so on, with parity that gives 24 codes. Therefore, the total number of codes is 464 codes, which can be fully represented by 9-bit codes. Indeed, in accordance with one aspect of the present invention, to ensure that parity and special code functions are passed onto the customers, the data may be transported transparently, as described above, for example, where 9-bit codes can fully represent the data.

In the manner described above, in accordance with the present invention, there is provided method and system for providing data transmission with transparency over the Gigabit Ethernet data stream which includes receiving the 10 bit code with a data rate of 1,250 Mbits/second from the encoded 8B/10B data and arbitrarily selecting 9 bit codes using a look-up translation table which can fully represent the 10 bit codes received. The translated 9 bit codes with a data rate of 1,125 Mbits/second is then provided to eight STS-3 inverse multiplexer which inverse multiplexes the received codes into eight STS-3 data streams each with a data rate of 155.52 Mbits/second + offset Δ which are then provided to the modem at the far end.

Various other modifications and alterations in the structure and method of operation of this invention will be apparent to those skilled in the art without departing from the scope and spirit of the invention. Although the invention has been described in connection with specific preferred embodiments, it should be understood that the invention as claimed should not be unduly limited to such specific embodiments. It is intended that the following claims define the scope of the present invention and that structures and methods within the scope of these claims and their equivalents be covered thereby.